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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2677	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,643	AKIMOTO ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3, 8-12,14,20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagata et al. (Pub. No.: US 2001/0028336 A1) in view of Miyazaki (US Patent No. 6, 344, 984 B1).

As to claim 1, Yamagata et al. teaches an image display apparatus comprising a display unit for displaying an image (See Fig. 1, item PNL, page 4, paragraph 0059) and a drive unit for driving this display unit See Fig. 1, items 30, page 4, paragraph 0059), the drive unit being connected by a plurality of signal lines (See Figs. 1, 2, item 4, paragraph 0064), display unit comprises a plurality of display pixels arranged in a matrix form (See Fig. 1, item PNL, paragraph 0004); drive unit comprises a ladder resistor (See Fig. 2, item 6); gray level voltage selecting means selectively connecting gray level voltage wires to plurality of signal lines (See Fig. 2, item 3, NLN, See page 4, paragraphs 0063-0064), wherein the number of analog gradation voltages matched with number of gray voltage wires (in reference – 64) gray level voltage wires (See page 4, paragraph 0063), and matches a number of a plurality of gray level voltage selectors of gray level voltage selecting means connected to the gray level voltage wires (See Fig. 2, item 3, NLN, See page 4, paragraphs 0063-0064).

Yamagata et al. does not show impedance converters each having an input connected to an output of the ladder resistor and gray level voltage wires constituting output lines connected to the impedance converters.

Miyazaki teaches impedance converters connected to an output of a ladder resistor (see Fig. 3, items R1-R5) and gray level voltage wires constituting output lines connected to the impedance converters (See Fig. 3, items A1-A5, V1-V5, from Col. 3, Line 58 to Col. 4, Line 2).

It would have been obvious to one of ordinary skill in the art at the time of invention use impedance converters connected to an output of the ladder and gray level voltage wires constituting output lines connected to the impedance converters as shown by Miyazaki in Yamagata et al. apparatus to reduce the power consumption (See Col. 2, Lines 35-39 in Miyazaki reference).

As to claim 20, Yamagata et al. teaches an image display terminal system, display unit comprising: a plurality of display pixels arranged in a matrix form to display an image (See Fig. 1, item PNL, paragraphs 0004, 0059); a group of signal lines provided for each column to transmit analog image signal and connected to the display pixels (See Figs. 1, 2, item 4, paragraph 0064), a drive circuit for driving pixels and the group of signal lines at prescribed timings (See Fig. 1, items 30, page 4, paragraph 0059), means for causing the display pixels to display an image in a prescribed sequence on the basis of inputted image display data (See Fig. 21, SEL1-SEL4, page 1, paragraph 0008), wherein: circuit has a ladder resistor and a plurality of gray voltage wires connected to an output of the ladder resistor (See Fig. 2, items 6, NLN); group of

signal lines are connected to the gray level voltage wires via a gray level voltage selector (See Figs. 1, 2, items 3, NLN, See page 4, paragraphs 0063-0064), the number of analog gradation voltages being matched with number of gray voltage wires (in He et al. reference – 64) gray level voltage wires (See page 4, paragraph 0063), and a gray level voltage selector connected to the gray level voltage wires (See Fig. 2, item 3, NLN, See page 4, paragraphs 0063-0064).

Yamagata et al. does not show impedance converters each having an input connected to an output of the ladder resistor and gray level voltage wires constituting output lines connected to the impedance converters.

Miyazaki teaches impedance converters connected to an output of a ladder resistor (see Fig. 3, items R1-R5) and gray level voltage wires constituting output lines connected to the impedance converters (See Fig. 3, items A1-A5, V1-V5, from Col. 3, Line 58 to Col. 4, Line 2).

It would have been obvious to one of ordinary skill in the art at the time of invention use impedance converters connected to an output of the ladder and gray level voltage wires constituting output lines connected to the impedance converters as shown by Miyazaki in Yamagata et al. apparatus to reduce the power consumption (See Col. 2, Lines 35-39 in Miyazaki reference).

Miyazaki and Yamagata et al. do not show the gray level voltage selector and the gray level voltage wires are provided over a single substrate. It is a common trend to integrate electronic display and controlling circuits on the substrate of the display in order to reduce costs and to improve the driving speed of display. Therefore, the skilled

person would also place voltage selector and the gray level voltage wires on the substrate of the display as mention in claim 20, without the exercise of inventive skill.

As to claims 2-3, Yamagata et al. teaches gray level voltage selector (See Fig. 2, item 3) connected to plurality of signal lines (See Figs. 1, items 30, PNL, See page 4, paragraphs 0063-0064).

As to claim 8, Miyazaki teaches liquid crystal display device (See Col. 1, Lines 6-10).

Miyazaki does not show liquid crystal in region between the pixel electrode and the counter electrode.

It would have been obvious if not inherent to one of ordinary skill in the art at the time of invention to use LC material in Miyazaki and Yamagata et al. in region between the pixel electrode and the counter electrode.

As to claim 9, Yamagata et al. teaches a gray level voltage selector is configured by an analog switch using a field effect transistor (See Fig. 2, item Tr, in description See page 4, paragraph 0063).

Miyazaki and Yamagata et al. do not disclose ladder resistor, voltage selector and impedance converters are configured by a polycrystalline Si and on the same substrate. It is a common trend to integrate electronic display and controlling circuits on the substrate of the display in order to reduce costs and to improve the driving speed of display. Therefore, the skilled person would also configured ladder resistor, voltage selector and impedance converters by a polycrystalline Si and on the same substrate of the display as mention in claims 10-12, without the exercise of inventive skill.

As to claim 14, Yamagata et al. teaches ladder resistor is a pair of resistors group, one each for positive voltage gray level generation and inverted polarity gray level generation (See Fig. 2, item 6, in description See page 4, paragraph 0063).

As to claims 21-22, Miyazaki teaches impedance converters are buffer amplifiers (voltage followers)(See Fig. 3, items A2-A5, Col. 3, Lines 58-65).

2. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki and Yamagata et al. in view of Nakajima et al. (US Patent No. 6, 181, 314 B1).

Miyazaki and Yamagata et al. do not show offset canceling unit for detecting and eliminating any offset voltage between input and output.

Nakajima et al. teaches offset canceling unit for detecting and eliminating any offset voltage between input and output (See Fig. 3, items 23-27, in description See from Col. 3, Line 44 to Col. 4, Line 58).

It would have been obvious to one of ordinary skill in the art at the time of invention use a offset canceling unit as shown by Nakajima et al. in Miyazaki and Yamagata et al. apparatus in order to provide an improved circuit in LCD device (See Col. 1, Line 66-67 in Nakajima et al. reference).

3. Claims 4-5, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki and Yamagata et al. in view of Morita (US Patent No. 6,366,065 B1).

As to claims 4-5, Yamagata et al. and Miyazaki do not show impedance converters configured by differential amplifying circuit using field-effect transistors.

Morita teaches impedance converters configured by differential amplifying circuit using field-effect transistors (See Fig. 10, 12, items 72, QP, in description See Col. 10, Lines 1-9).

It would have been obvious to one of ordinary skill in the art at the time of invention use a differential amplifying circuit using field-effect transistors as shown by Morita in Miyazaki and Yamagata et al. apparatus as part of D-A converter instead of the output buffers.

As to claim 7, Miyazaki and Yamagata et al. do not show means for suspending the functioning of the impedance converters and circuits for short-circuiting the input and output terminals of the impedance converters.

Morita teaches means for suspending the functioning of the impedance converters and circuits for short-circuiting the input and output terminals of the impedance converters (See Fig. 5, items 72, Q2, in description See Col. 6, Lines 39-59).

It would have been obvious to one of ordinary skill in the art at the time of invention use a differential amplifying circuit using field-effect transistors as shown by Morita in Miyazaki and Yamagata et al. apparatus as part of D-A converter instead of the output buffers.

4. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki and Yamagata et al. in view of Negishi et al. (US Patent No. 5, 528, 241).

Miyazaki and Yamagata et al. do not show a ladder resistor is configured as one resistor.

Negishi et al. teaches ladder resistor is configured as one resistor (See Fig. 2, item20, in description See from Col. 2, Line 64 to Col. 3, Line 32 and Abstract).

It would have been obvious to one of ordinary skill in the art at the time of invention use a ladder resistor is configured as one resistor as shown by Negishi et al. in Miyazaki and Yamagata et al. apparatus in order to provide an improved circuit in LCD device.

5. Claims 15-16, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagata et al. in view of Miyazaki and Kane (US Patent No. 6,229,508 B1).

As to claim 16, Yamagata et al. teaches an image display apparatus driving method for displaying an image (See Fig. 1, item PNL, page 4, paragraph 0059) by writing analog image signal voltages via signal lines into pixel capacitances of individual pixels in a display unit (See Figs. 1, 2, item 4, paragraph 0064), wherein the analog image signal voltages are written into an image display apparatus having a drive unit (See Fig. 1, item PNL, paragraph 0004); including a ladder resistor (See Fig. 2, item 6); gray level voltage selecting means selectively connecting gray level voltage wires to plurality of signal lines (See Fig. 2, item 3, NLN, See page 4, paragraphs 0063-0064), the number of analog gradation voltages being matched with number of gray voltage wires (in reference – 64) gray level voltage wires (See page 4, paragraph 0063), and a

gray level voltage selector connected to the gray level voltage wires (See Fig. 2, item 3, NLN, See page 4, paragraphs 0063-0064).

Yamagata et al. does not show impedance converters each having an input connected to an output of the ladder resistor and gray level voltage wires constituting output lines connected to the impedance converters.

Miyazaki teaches impedance converters connected to an output of a ladder resistor (see Fig. 3, items R1-R5) and gray level voltage wires constituting output lines connected to the impedance converters (See Fig. 3, items A1-A5, V1-V5, from Col. 3, Line 58 to Col. 4, Line 2).

It would have been obvious to one of ordinary skill in the art at the time of invention use impedance converters connected to an output of the ladder and gray level voltage wires constituting output lines connected to the impedance converters as shown by Miyazaki in Yamagata et al. apparatus to reduce the power consumption (See Col. 2, Lines 35-39 in Miyazaki reference).

Miyazaki and Yamagata et al. do no show the analog image signal voltages are written in three separate phases when analog image signal voltages are to be written onto the signal lines.

Kane teaches three separate phases when the analog image signal voltages are to be written onto the signal line (See Figs. 5-6, items 550,530,510, PRECHRGE, AUTOZERO,WRITE DATA, in description See from Col. 5, Line 43 to Col. 6, Line 50).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the driver as shown by Kane in Miyazaki and Yamagata et al. method in order to improve brightness uniformity (See Col. 2, Lines 9-10 in Kane reference).

As to claim 19, Yamagata et al. teaches a driving method for an image display terminal system, display unit comprising: a plurality of display pixels arranged in a matrix form to display an image (See Fig. 1, item PNL, paragraphs 0004, 0059); a group of signal lines provided for each column to transmit analog image signal and connected to the display pixels (See Figs. 1, 2, item 4, paragraph 0064), a drive circuit for driving pixels and the group of signal lines at prescribed timings (See Fig. 1, items 30, page 4, paragraph 0059), means for causing the display pixels to display an image in a prescribed sequence on the basis of inputted image display data (See Fig. 21, SEL1-SEL4, page 1, paragraph 0008), wherein: drive circuit has a ladder resistor and a plurality of gray voltage wires connected to an output of the ladder resistor (See Fig. 2, items 6, NLN); group of signal lines are connected to the gray level voltage wires via a gray level voltage selector (See Figs. 1, 2, items 3, NLN, See page 4, paragraphs 0063-0064), the number of analog gradation voltages being matched with number of gray voltage wires (in reference – 64) gray level voltage wires (See page 4, paragraph 0063), and a gray level voltage selector connected to the gray level voltage wires (See Fig. 2, item 3, NLN, See page 4, paragraphs 0063-0064).

Yamagata et al. does not show impedance converters each having an input connected to an output of the ladder resistor and gray level voltage wires constituting output lines connected to the impedance converters.

Miyazaki teaches impedance converters connected to an output of a ladder resistor (see Fig. 3, items R1-R5) and gray level voltage wires constituting output lines connected to the impedance converters (See Fig. 3, items A1-A5, V1-V5, from Col. 3, Line 58 to Col. 4, Line 2).

It would have been obvious to one of ordinary skill in the art at the time of invention use impedance converters connected to an output of the ladder and gray level voltage wires constituting output lines connected to the impedance converters as shown by Miyazaki in Yamagata et al. apparatus to reduce the power consumption (See Col. 2, Lines 35-39 in Miyazaki reference).

Miyazaki and Yamagata et al. do not show the gray level voltage selector and the gray level voltage wires are provided over a single substrate.

Miyazaki and Yamagata et al. do not show the gray level voltage selector and the gray level voltage wires are provided over a single substrate. It is a common trend to integrate electronic display and controlling circuits on the substrate of the display in order to reduce costs and to improve the driving speed of display. Therefore, the skilled person would also voltage selector and the gray level voltage wires on the substrate of the display as mention in claim 20, without the exercise of inventive skill.

Miyazaki and Yamagata et al. do no show the analog image signal voltages are written in three separate phases when analog image signal voltages are to be written onto the signal lines.

Kane teaches three separate phases when the analog image signal voltages are to be written onto the signal line (See Figs. 5-6, items 550,530,510, PRECHRGE, AUTOZERO,WRITE DATA, in description See from Col. 5, Line 43 to Col. 6, Line 50).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the driver as shown by Kane in Miyazaki and Yamagata et al. method in order to improve brightness uniformity (See Col. 2, Lines 9-10 in Kane reference).

As to claim 15, Miyazaki and Yamagata et al. do not show a luminescent type of display pixels controlled by entered analog image signal and having a light emitting function for displaying an image with luminescence generated by a current flowing between a positive and a negative electrode.

Kane teaches a luminescent type of display pixels controlled by entered analog image signal and having a light emitting function for displaying an image with luminescence generated by a current flowing between a positive and a negative electrode (See Figs. 1-3, item 304, in description See Col. 3, Lines 28-62).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the driver as shown by Kane in Miyazaki and Yamagata et al. apparatus to incorporate a LED (OLED) pixel structure (See Col.2, Lines 9-12 in the Kane reference).

As to claim 18, Kane teaches signal lines are provided with voltage resetting circuits, and analog image signal voltages are written in three separate phases after the voltages of the signal lines are reset in advance by the resetting circuits (See Figs. 5-6,

items 550,530,510, PRECHRGE, AUTOZERO,WRITE DATA, in description See Col. 6, Lines 15 and 36).

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki, Yamagata et al, Kane as applied to claim 16 above, and further in view of Nakajima et al.

Miyazaki, Yamagata et al. do not show display driving method for displaying an image by writing analog image signal voltages via signal lines into pixel capacitances of individual pixels in a display unit, wherein the analog image signal voltages are written in two separate phases when the analog image signal voltages are to be written onto the signal line.

Nakajima et al. teaches display driving method for displaying an image by writing analog image signal voltages via signal lines into pixel capacitances of individual pixels in a display unit, wherein the analog image signal voltages are written in two separate phases when the analog image signal voltages are to be written onto the signal line (See Figs. 3-4, items 21-26,T1,T2, in description See from Col. 3, Line 45 to Col. 5, Line 7).

It would have been obvious to one of ordinary skill in the art at the time of invention use a first and second phases as shown by Nakajima et al., Miyazaki and Yamagata et al. apparatus in order to provide an improved circuit in LCD device (See Col. 1, Line 66-67 in Nakajima et al. reference).

Nakajima et al, Miyazaki, and Yamagata et al. do not show the third phase.

Kane teaches three separate phases when the analog image signal voltages are to be written onto the signal line (See Figs. 5-6, items 550,530,510, PRECHRGE, AUTOZERO,WRITE DATA, in description See from Col. 5, Line 43 to Col. 6, Line 50).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the driver as shown by Kane in Nakajima et al, Miyazaki and Yamagata et al. apparatus in order to improve brightness uniformity (See Col. 2, Lines 9-10 in Kane reference).

Response to Arguments

7. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS
02.15.06

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